OV6650 Color CMOS CIF (352 x 288) CAMERACHIP™
OV6151 B&W CMOS CIF (352 x 288) CAMERACHIP™

General Description

The OV6650 (color) and OV6151 (black and white) CMOS CAMERACHIPS™ are single-chip video/imaging camera devices designed to provide a high level of functionality in a single, small-footprint package. The devices incorporate a 352 x 288 image array capable of operating at up to 30 frames per second (fps). Proprietary sensor technology utilizes advanced algorithms to cancel Fixed Pattern Noise (FPN), eliminate smearing, and drastically reduce blooming. All required camera functions including exposure control, gamma, gain, white balance, color matrix, color saturation, hue control, windowing, and more, are programmable through the SCCB interface. The device can be programmed to provide image output in different 8-bit formats.

Features

- 108,472 total pixels
- 1/7" optical size
- Wide dynamic range, anti-blooming, zero smearing
- Progressive Scan
- Electronic exposure/gain/white balance control
- Image quality controls:
  - Brightness
  - Gamma
  - Saturation
  - Sharpness
  - Hue
- Internal synchronization
- Line exposure option
- SCCB programmable:
  - Color saturation
  - Brightness
  - Hue
  - Windowing
  - White balance
  - Exposure time
  - Gain

Ordering Information

Product	Package
OV06650-K06A (Color)	CSP-22
OV06151-K06A (B&W with microlens)	CSP-22

Applications

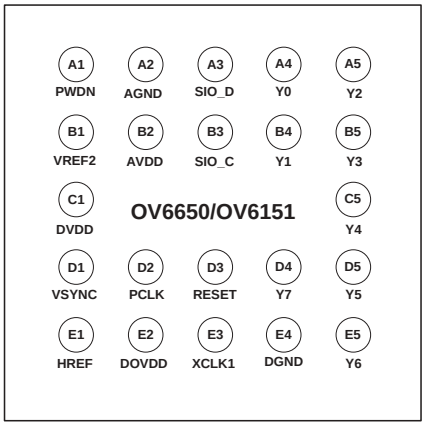
- Picture Phones
- Cellular Phones
- Toys
- PDAs
- PC Multimedia

Key Specifications

Array Size		352 x 288 (CIF)
Power Supply	**Core**	2.5VDC ± 10%
	Analog	2.5VDC ± 4%
	I/O	2.25V to 3.3V
Power Requirements	**Active**	20 mW
	Standby	30 µW
Temperature Range	**Operation**	0°C to 70°C
	Stable Image	0°C to 50°C
Output Formats		• YUV/YCbCr 4:2:2 • RGB 4:2:2 • Raw RGB Data
Lens Size		1/7"
Maximum Image Transfer Rate		30 fps
Sensitivity	**B&W**	2.20 V/Lux-sec
	Color	1.12 V/Lux-sec
S/N Ratio		46 dB
Dynamic Range		62 dB
Scan Mode		Progressive
Maximum Exposure Interval		312 x t_{ROW}
Gamma Correction		0.45
Pixel Size		5.6 µm x 5.6 µm
Dark Current		30 mV/s
Well Capacity		63 Ke
Fixed Pattern Noise		< 0.03% of $V_{PEAK-TO-PEAK}$
Image Area		1.97 mm x 1.61 mm
Package Dimensions		3425 µm x 3485 µm

Note: All specifications at 5,000°K ambient light

Figure 1 OV6650/OV6151 Pin Diagram (Top View)



Functional Description

Figure 2 shows the functional block diagram of the OV6650/OV6151 image sensor. The OV6650/OV6151 includes:

- Image Sensor Array (352 x 288 resolution)
- Timing Generator
- Analog Processing Block
- A/D Converters
- Output Formatter
- Digital Video Output Control
- SCCB Interface

Figure 2 OV6650/OV6151 Functional Block Diagram

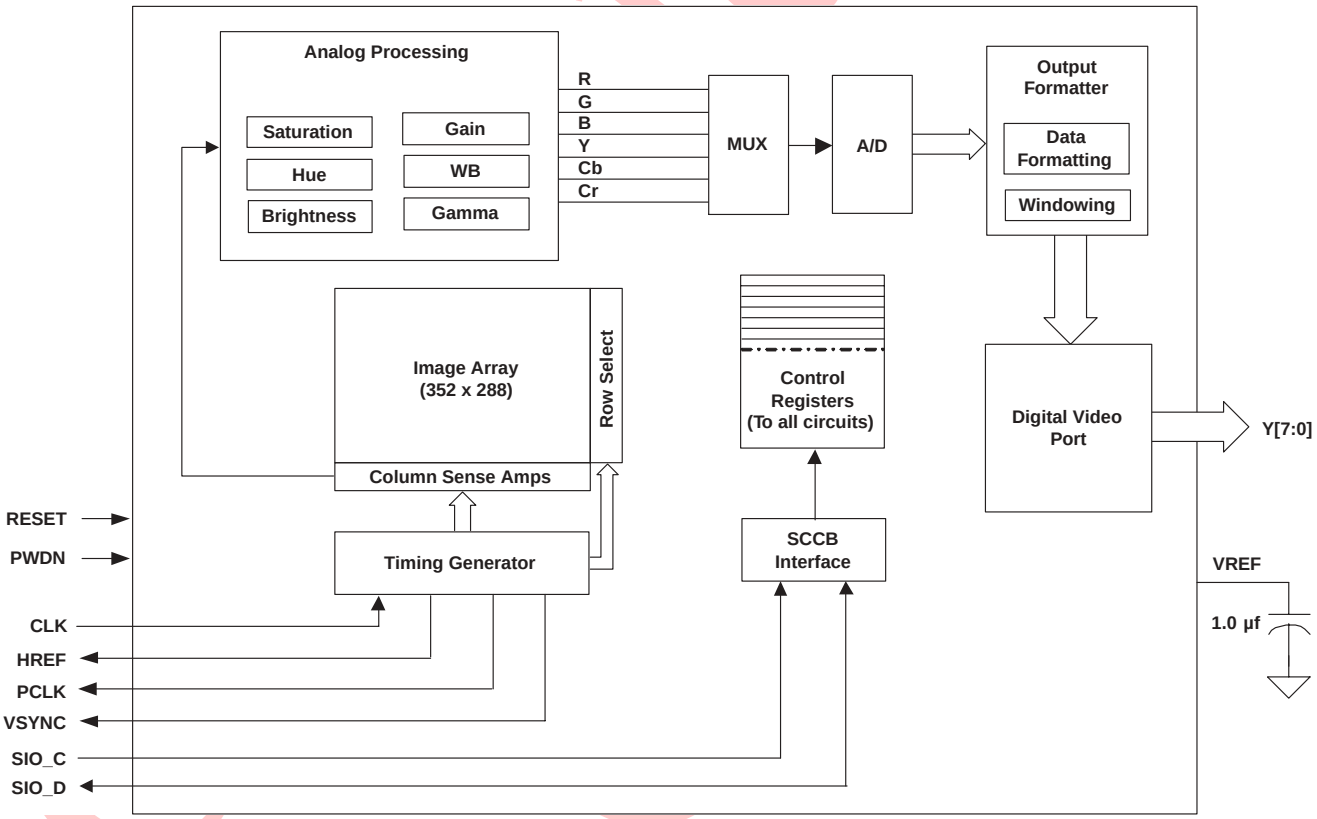
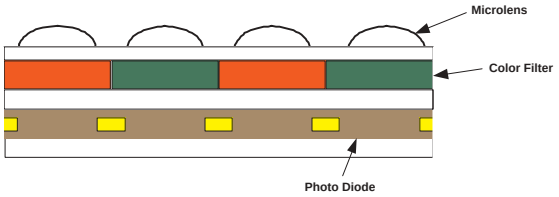


Image Sensor Array

The OV6650/OV6151 CAMERACHIPS has an active image array size of 352 columns x 288 rows (101,376 pixels). However, the full array contains 364 columns and 298 rows, with the extra 10 rows used for black-level calibration (“Optical Black”) and color interpolation information. Figure 3 shows a cross-section of the image sensor array.

Figure 3 Image Sensor Array



Timing Generator

In general, the timing generator controls these functions:

- Array control and frame generation (CIF and QCIF outputs)
- Internal timing signal generation and distribution
- Frame rate timing
- Automatic Exposure Control (AEC)
- External timing outputs (VSYNC, HREF and PCLK)

Analog Processing Block

This block performs all analog image functions including:

- Automatic Gain Control (AGC)
- Automatic White Balance (AWB)
- Image quality controls including:
  - Color saturation
  - Hue
  - Gamma
  - Sharpness (edge enhancement)
  - Anti-blooming
  - Zero smearing

A/D Converters

After the Analog Processing Block, the color channel data signal is fed to one 8-bit Analog-to-Digital (A/D) converter via the multiplexers. The A/D converter operates at speeds up to 8MHz and is fully synchronous to the pixel rate (actual conversion rate is related to the frame rate).

In addition to the A/D conversion, this block also has the following functions:

- Digital Black-Level Calibration (BLC)
- Optional U/V channel delay and average
- Additional A/D range controls

In general, the combination of the A/D Range Multiplier and A/D Range Control sets the A/D range and maximum value to allow the user to adjust the final image brightness as a function of the individual application.

Output Formatter

This block controls all output and data formatting required prior to sending the image out. The OV6650/OV6151 supports formats that include YUV 4:2:2, RGB 4:2:2, Raw RGB, and Nibble mode for both CIF and QCIF.

Digital Video Output Control

There are two SCCB bits to increase I_{OL} / I_{OH} drive current and can be adjusted as a function of the customer’s loading:

SCCB Interface

The Serial Camera Control Bus (SCCB) interface controls the CAMERACHIP operation. Refer to *OmniVision Technologies Serial Camera Control Bus (SCCB) Specification* for detailed usage of the serial control port.

Pin Description

Table 1 Pin Description

Pin Location	Name	Pin Type	Function/Description
A1	PWDN	Function (default = 0)	Power Down Mode Selection 0: Normal mode 1: Power down mode
A2	AGND	Power	Analog ground
A3	SIO_D	I/O	SCCB serial interface data I/O
A4	Y0	Output	YUV video component output bit[0]
A5	Y2	Output	YUV video component output bit[2]
B1	VREF2	V_{REF}	Internal voltage reference. Connect to ground through 1µF capacitor
B2	AVDD	Power	Analog power supply (+2.5 VDC)
B3	SIO_C	Input	SCCB serial interface clock input
B4	Y1	Output	YUV video component output bit[1]
B5	Y3	Output	YUV video component output bit[3]
C1	DVDD	Power	Power supply (+2.5 VDC) for digital output drive
C5	Y4	Output	YUV video component output bit[4]
D1	VSYNC	Output	Vertical sync output
D2	PCLK	Output	Pixel clock output
D3	RESET	Function (default = 0)	Chip reset, active high
D4	Y7	Output	YUV video component output bit[7]
D5	Y5	Output	YUV video component output bit[5]
E1	HREF	Output	HREF output
E2	DOVDD	Power	Digital power supply (+2.5 to 3.3VDC)
E3	XCLK1	Input	Crystal clock input
E4	DGND	Power	Digital ground
E5	Y6	Output	YUV video component output bit[6]

Electrical Characteristics

Table 2 Absolute Maximum Ratings

Ambient Storage Temperature		-40ºC to +125ºC
Supply Voltages (with respect to Ground)	**V_{DD-A}**	3V
	V_{DD-C}	3V
	V_{DD-IO}	4V
All Input/Output Voltages (with respect to Ground)		-0.3V to VDD_IO+1V
Lead Temperature, Surface-mount process		+230ºC
ESD Rating, Human Body model		±2000V

NOTE: Exceeding the Absolute Maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent device damage.

Table 3 DC Characteristics (0°C < T_A < 70°C)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD-A}	DC supply voltage – Analog	—	2.40	2.5	2.60	V
V_{DD-C}	DC supply voltage – Core	—	2.25	2.5	2.75	V
V_{DD-IO}	DC supply voltage – I/O	—	2.25	—	3.3	V
I_{DD-A}	Active (Operating) Current	See Note [a]		8		mA
$I_{DDS-SCCB}$	Standby Current	See Note [b]		1		mA
$I_{DDS-PWDN}$	Standby Current			10		µA
V_{IH}	Input voltage HIGH	CMOS	0.7 x V_{DD-IO}			V
V_{IL}	Input voltage LOW				0.3 x V_{DD-IO}	V
V_{OH}	Output voltage HIGH	CMOS (I_{OH} / I_{OL})	0.9 x V_{DD-IO}			V
V_{OL}	Output voltage LOW				0.1 x V_{DD-IO}	V
I_{OH}	Output current HIGH	See Note [c]	8			mA
I_{OL}	Output current LOW		15			mA
I_L	Input/Output Leakage	GND to V_{DD-IO}			± 1	µA

a. V_{DD-A} = V_{DD-C} = 2.5V, V_{DD-IO} = 3.0V
$I_{DDA} = \Sigma\{I_{DD-IO} + I_{DD-C} + I_{DD-A}\}$, f_{CLK} = 24MHz at 30 fps, no I/O loading

b. V_{DD-A} = V_{DD-C} = 2.5V, V_{DD-IO} = 3.0V
$I_{DDS:SCCB}$ refers to a SCCB-initiated Standby, while $I_{DDS:PWDN}$ refers to a PWDN pin-initiated Standby

c. Standard Output Loading = 25pF, 1.2KΩ to 3V

Table 4 Functional and AC Characteristics (0°C < T_A < 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
Functional Characteristics					
	A/D Differential Non-Linearity		± 1/2		LSB
	A/D Integral Non-Linearity		± 1		LSB
	AGC Range			21	dB
	Red/Blue Adjustment Range			12	dB
Inputs (PWDN, CLK, RESET)					
f_{CLK}	Input Clock Frequency	8	24	27	MHz
t_{CLK}	Input Clock Period	37	42	125	ns
$t_{CLK:DC}$	Clock Duty Cycle	45	50	55	%
$t_{S:RESET}$	Setting time after software/hardware reset			1	ms
$t_{S:REG}$	Settling time for register change (10 frames required)			300	ms
SCCB (SIO_C and SIO_D - see Figure 4)					
f_{SIO_C}	Clock Frequency			400	KHz
t_{LOW}	Clock Low Period	1.3			µs
t_{HIGH}	Clock High Period	600			ns
t_{AA}	SIO_C low to Data Out valid	100		900	ns
t_{BUF}	Bus free time before new START	1.3			µs
$t_{HD:STA}$	START condition Hold time	600			ns
$t_{SU:STA}$	START condition Setup time	600			ns
$t_{HD:DAT}$	Data-in Hold time	0			µs
$t_{SU:DAT}$	Data-in Setup time	100			ns
$t_{SU:STO}$	STOP condition Setup time	600			ns
t_R, t_F	SCCB Rise/Fall times			300	ns
t_{DH}	Data-out Hold time	50			ns
Outputs (VSYNC, HREF, PCLK, and Y[7:0] - see Figure 5, Figure 6, and Figure 7)					
t_{PDV}	PCLK[↓] to Data-out Valid			5	ns
t_{SU}	Y[7:0] Setup time	15			ns
t_{HD}	Y[7:0] Hold time	8			ns
t_{PHH}	PCLK[↓] to HREF[↑]	0		5	ns
t_{PHL}	PCLK[↓] to HREF[↓]	0		5	ns
AC Conditions:	• V_{DD}: V_{DD-A} = V_{DD-C} = 2.5V, V_{DD-IO} = 3.3V • Rise/Fall Times: I/O: 5ns, Maximum SCCB: 300ns, Maximum • Input Capacitance: 10pf • Output Loading: 25pF, 1.2KΩ to 3V • f_{CLK}: 24MHz				

Timing Specifications

Figure 4 SCCB Timing Diagram

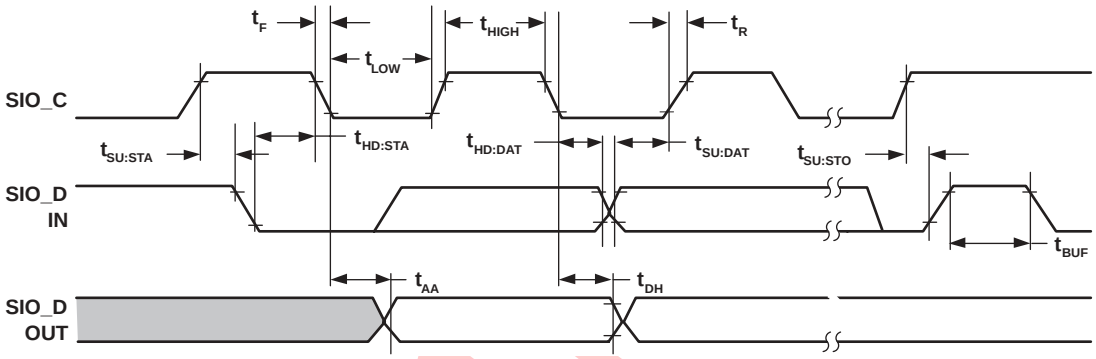


Figure 5 Row Output Timing Diagram

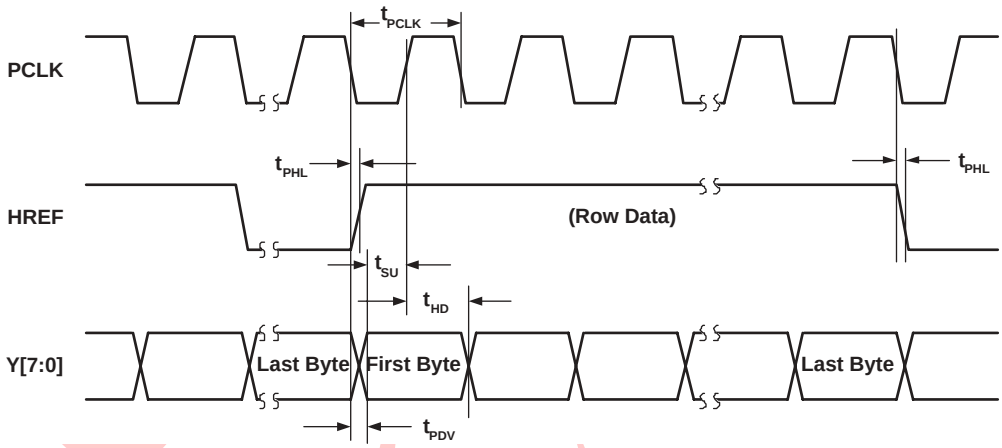


Figure 6 CIF Frame Timing Diagram

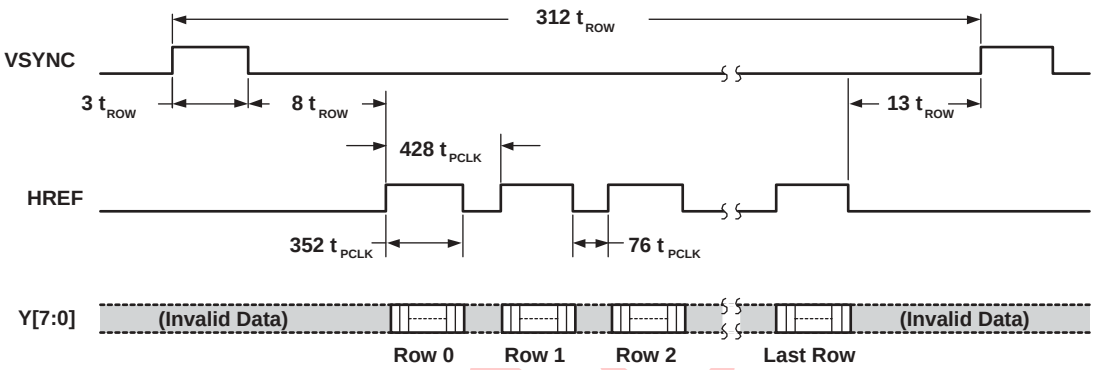
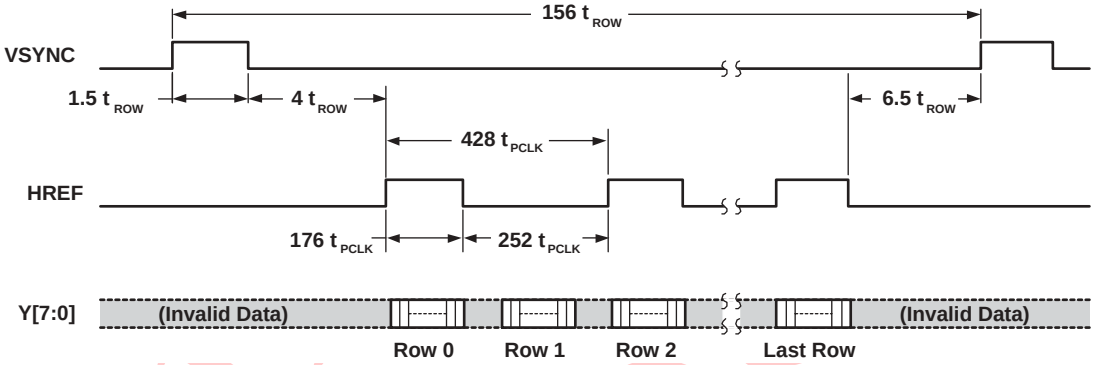


Figure 7 QCIF Frame Timing Diagram



Note: As the RGB, YUV and YCbCr formats use the Bayer pattern for interpolation, the first row transferred out on the Y[7:0] bus will be invalid, as there is no row above Row #1 to provide the 'pair data' required. Because of this, the OV6650 does not enable the HREF signal during the first row read (shown above in the 'invalid data' zone).

Register Set

Table 5 provides a list and description of the Device Control registers contained in the OV6650/OV6151. The device slave addresses for the OV6650/OV6151 are C0 for write and C1 for read.

Table 5 SCCB Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
00	GAIN	00	RW	AGC – Gain control gain setting • Range: [00] to [3F]
01	BLUE	80	RW	AWB – Blue channel gain setting • Range: [00] to [FF] ***Note:*** *This function is not available on the B&W OV6151.*
02	RED	80	RW	AWB – Red channel gain setting • Range: [00] to [FF] ***Note:*** *This function is not available on the B&W OV6151.*
03	SAT	88	RW	Image Format – Color saturation value Bit[7:4]: Saturation value • Range: [0] to [F] Bit[3:0]: Reserved ***Note:*** *This function is not available on the B&W OV6151.*
04	HUE	10	RW	Image Format – Color hue control Bit[7:6]: Reserved Bit[5]: Hue Enable Bit[4:0]: Hue setting ***Note:*** *This function is not available on the B&W OV6151.*
05	RSVD	XX	–	Reserved
06	BRT	80	RW	ABC – Brightness setting • Range: [00] to [FF]
07-09	RSVD	XX	–	Reserved
0A	PIDH	66	R	Product ID number - high 8 bits (Read only)
0B	PIDL	50	R	Product ID number - low 8 bits (Read only)
0C-0F	RSVD	XX	–	Reserved
10	AECH	4D	RW	Exposure Value
11	CLKRC	00	RW	Data Format and Internal Clock Bit[7:6]: Input system clock 00: 8 MHz 01: 12 MHz 10: 16 MHz 11: 24 MHz Bit[5:0]: Internal Clock Pre-Scalar • Range: [0 0000] to [1 1111]

Table 5 SCCB Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
12	COMA	00	RW	Common Control A Bit[7]: SCCB – Register Reset 0: No change 1: Reset all registers to default values Bit[6]: Data Format – ITU-656 Format Enable Bit[5]: Output format – resolution 0: CIF (352 x 288) 1: QCIF (176 x 144) Bit[4]: Output format – RGB output select 0: RGB 1: Raw RGB Bit[3]: Output Format – Output Channel Select 0: YUV/YCbCr 1: RGB/Raw RGB Bit[2]: Device select 0: OV6650 1: OV6151 (B&W mode) Bit[1]: Data format – UV sequence exchange 0: U Y V Y U Y V Y 1: V Y U Y V Y U Y Bit[1:0]: Data format – YUV sequence exchange 0: U Y V Y U Y V Y 1: Y U Y V Y U Y V
13	COMB	5F	RW	Common Control B Bit[7]: Vertical flip Bit[6]: Gamma function ON for RGB/color channel Bit[5]: Mirror image Bit[4]: AEC – Band filter enable Bit[3]: Fast AEC/AGC Bit[2]: AWB enable Bit[1]: AGC enable Bit[0]: AEC enable
14	COMC	41	RW	Common Control C Bit[7]: Drop one frame when AEC step is bigger than 24 lines Bit[6]: Minimum Exposure time can be less than 1 line Bit[5]: Night mode enable – When this mode is ON, the frame rate is adjusted automatically to meet low light conditions. The maximum frame change is based on COMD[1:0] Bit[4]: AEC big step enable – If this option is ON, COMC[7] will usually need to be turned ON. Bit[3:2]: AWB update step selection Bit[1:0]: AEC – Max gain selection x0: 2x 01: 4x 11: 8x

Table 5 SCCB Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
15	COMD	01	RW	Common Control D Bit[7]: Band filter option – Enables 4 MHz input clock to synchronize light frequency Bit[6]: AWB sensitivity threshold option 1: Less sensitive, more stable Bit[5]: Reserved Bit[4]: Enables AWB fast mode – AWB updated every frame Bit[3]: AWB update step selection 0: Enables AWB updating every 4 frames 1: Enables AWB updating every 16 frames Bit[2]: Disables AWB clock when AEC/AGC is adjusting Bit[1:0]: Maximum frame change used for night mode 00: No frame rate change 01: Maximum 1/2 frame rate change 10: Maximum 1/4 frame rate change 11: Maximum 1/8 frame rate change
16	COML	02	RW	Common Control K Bit[7]: A/D one channel select – When using YUV 4:2:2 or RGB 4:2:2 format, this option must be turned ON. For Raw RGB output, this register should be set to "0" since in Raw data mode, A/D one channel is selected automatically Bit[6]: ADBLC select 0: ADBLC only for ADC 1: ADBLC for whole channel Bit[5]: Output optical black data Bit[4]: HREF selection 0: HREF 1: CC656 Bit[3]: Data bus tri-state Bit[2]: VSYNC dropping enable 0: Always output VSYNC 1: Allow VSYNC dropping Bit[1]: VSYNC drop select – only effective when COML[2] 0: Do not drop VSYNC when frame is dropped 1: Drop VSYNC when frame is dropped Bit[0]: Freeze AEC/AGC clocks
17	HSTART	24	RW	Output Format – Horizontal Frame (HREF Column) Start
18	HSTOP	D4	RW	Output Format – Horizontal Frame (HREF Column) Stop
19	VSTRT	04	RW	Output Format – Vertical Frame (Row) Start
1A	VSTOP	94	RW	Output Format – Vertical Frame (Row) Stop
1B	PSHFT	00	RW	Data Format – Pixel Delay Select (Delays timing of the Y[7:0] data relative to HREF in pixel units) • Range: [00] (No delay) to [FF] (256 pixel delay)
1C	MIDH	7F	R	Manufacturer ID Byte – High (Read only = 0x7F)
1D	MIDL	A2	R	Manufacturer ID Byte – Low (Read only = 0xA2)
1E	HSYNCS	0F	RW	Output format – Horizontal sync start

Table 5 SCCB Register List

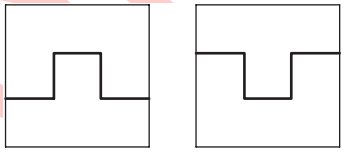
Address (Hex)	Register Name	Default (Hex)	R/W	Description
1F	HSYNCE	2F	RW	Output format – Horizontal sync end
20	COME	80	RW	Common Control E Bit[7]: Enable Optical Black Level Calibration Bit[6:5]: Reserved Bit[4]: Sleep mode Bit[3:0]: Reserved
21	YOFF	80	RW	Y Offset Bit[7:0]: Y offset value
22	UOFF	80	RW	U Offset Bit[7:0]: U offset value
23	VOFF	80	RW	V Offset Bit[7:0]: V offset value
24	AEW	C0	RW	AGC/AEC – Stable Operating Region – Upper Limit
25	AEB	80	RW	AGC/AEC – Stable Operating Region – Lower Limit
26	COMF	01	RW	Common Control F Bit[7:6]: When A/D one channel, swap Y and U/V selection Bit[6]: Swap U/V BLC window Bit[5]: Data Format – Output Data MSB/LSB Swap Enable (LSB → MSB (Y[7]) and MSB → LSB (Y[0]) Bit[4]: Data Format – HREF Polarity 0: HREF Positive 1: HREF Negative  POS NEG Bit[3]: Data format – Output HSYNC on HREF pin enable Bit[2]: Enables COMF[1] Bit[1]: Reverse ADCK2 for match UV sequence (in YUV and AD1CH mode) Bit[0]: When band filter is ON, exposure can reach under minimum exposure time.
27	COMG	54	RW	Common Control G Bit[7]: Edge half Bit[6]: Edge enhancement enable Bit[5:4]: Edge threshold • Range: [00] (most sensitive) to [11] (least sensitive) Bit[3:2]: Edge selection • Range: [00] to [11] (increase edge enhancement) Bit[1]: Edge high Bit[0]: Delay Y sequence instead of UV

Table 5 SCCB Register List

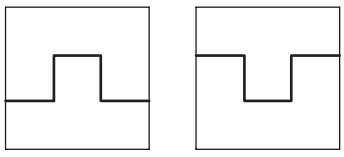
Address (Hex)	Register Name	Default (Hex)	R/W	Description
28	COMH	08	RW	Common Control H Bit[7]: In Raw RGB mode, switch R/B selection clocks for R/B average Bit[6:5]: Reserved Bit[4]: Output U/V average Bit[3:2]: HREF delay MSB Bit[1:0]: Reserved
29	COMI	80	RW	Common Control I Bit[7]: ADBLC on Bit[6]: HSYNC drop select – Only effective when HREFO outputs HSYNC 0: Drops HSYNC when frame is dropped 1: Never drops HSYNC Bit[5]: Bypass RGB matrix Bit[4]: A/D offset manual mode Bit[3]: Frame output data (only for Y/G) Bit[2]: Reserved Bit[1]: Disables Y BLC window Bit[0]: Reserved
2A	RSVD	00	–	Reserved
2B	FRARL	00	RW	Data Format – Frame Rate Adjust (by inserting dummy pixels) Setting LSB FRA[8:0] = MSB + LSB = COMK[5] + FRARL[7:0]
2C	COMJ	08	RW	Common Control J Bit[7:6]: Adjust crystal's for driving gates Bit[5]: PCLK output gated by HREF enable Bit[4]: Data format – Y[7:0] PCLK reference edge 0: Y[7:0] data out on PCLK falling edge 1: Y[7:0] data out on PCLK rising edge Bit[3]: Reserved Bit[2]: Nibble mode – only 4 MSB used, PCLK double Bit[1:0]: Data Format – HSYNC/VSYNC Polarity 00: HSYNC = NEG VSYNC = POS 01: HSYNC = NEG VSYNC = NEG 10: HSYNC = POS VSYNC = POS 11: HSYNC = POS VSYNC = POS  POS NEG

Table 5 SCCB Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
2D	COMK	00	RW	Common Control K Bit[7:6]: Adjust IO pads drive power Bit[5]: Frame rate adjust HSB (see "FRARL" on page 13) Bit[4:3]: Delay option (for UV sequence or Y sequence) • Range: [00] to [11] (increases delay) Bit[2]: Reserved Bit[1:0]: AECL[1:0]
2E	AVGY	00	RW	Average Y or G
2F	REF0	9C	–	Reserved
30	REF1	00	–	Reserved
31	REF2	00	–	Reserved
32	FRAJH	00	RW	Frame adjust MSB
33	FRAJL	00	RW	Frame adjust LSB FRAJ[15:0] is the value inserted to vertical SYNC. Each bit represents 1 line frame. When COMC[5] is high, FRAJ[15:0] is automatically updated.
34	FACT	F4	RW	Fast AGC/AEC Control Zone – High 4 bits is high 4 bits of top limit and low 4 bits is high 4 bits of bottom limit
35	L1AEC	00	RW	Exposure time value when L1AEC is enabled and exposure time is less than 1 line. This register automatically updates when auto function is ON.
36	AVGU	00	RW	Average value for U or B
37	AVGV	00	RW	Average value for V or R
38-5F	RSVD	XX	–	Reserved
60	SPCB	06	RW	Signal Process Control B Bit[7]: AGC – 1.5x Multiplier (Pre-amplifier) Enable Bit[6]: Analog current half Bit[5]: Gev/God switch instead of average for color channel (when output RGB) or G (when output RGB) Bit[4]: Gev/God switch instead of average for Y channel Bit[3:2]: R channel pre gain Bit[1:0]: B channel pre gain
61	SPCC	60	RW	Signal Process Control C Bit[7:4]: Reserved Bit[3]: Enable brightness control for RGB Bit[2]: Brightness control range and step half Bit[1:0]: Color Matrix – YUV/YCbCr Coefficient Select (Sets coefficients for RGB to YUV/YCbCr conversion) 0.59G + 0.31R + 0.11B → Y α(B – Y) → Y and Cb β(R – Y) → V and Cb Bits α β Format 00 1.000 1.000 YUV 01 0.938 0.838 – 10 0.563 0.713 YCbCr 11 0.500 0.877 –

Table 5 SCCB Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
62	GAM1	12	RW	RGB Gamma Control
63	GAM2	91	RW	Gamma Control Bit[7]: Y Gamma enable Bit[6:0]: Reserved
64	GAM3	88	RW	Y Gamma Control
65	SPCD	00	RW	Signal Process Control D Bit[7]: Bypass auto zero for RGB Bit[6]: Bypass UV channel BLC Bit[5]: Bypass Y channel BLC Bit[4]: Enable Even/Odd noise compensation Bit[3:0]: Even/Odd noise compensation value
66-67	RSVD	XX	–	Reserved
68	SPCE	08	RW	Signal Process Control E Bit[7:4]: Reserved Bit[3:2]: ADC current control Bit[1]: Reserved Bit[0]: Power down ADC when not in use (only for Raw data format)
69	ADCL	04	RW	ADC Control Bit[7:4]: Reserved Bit[3]: ADC range control by pre gain Bit[2:0]: ADC range control by reference
6A-6B	RSVD	XX	–	Reserved
6C	RMCO	11	RW	Color Matrix – RGB Crosstalk Compensation – R Channel ***Note:*** *This function is not available on the B&W OV6151.*
6D	GMCO	01	RW	Color Matrix – RGB Crosstalk Compensation – G Channel ***Note:*** *This function is not available on the B&W OV6151.*
6E	BMCO	06	RW	Color Matrix – RGB Crosstalk Compensation– B Channel ***Note:*** *This function is not available on the B&W OV6151.*
6F-7D	RSVD	XX	–	Reserved
NOTE: All other registers are factory-reserved. Please contact OmniVision Technologies for reference register settings.				

Package Specifications

The OV6650/OV6151 uses a 22-ball Chip Scale Package (CSP). Refer to Figure 8 for package information, Table 6 for package dimensions and Figure 9 for the array center on the chip.

Figure 8 OV6650/OV6151 Package Specifications

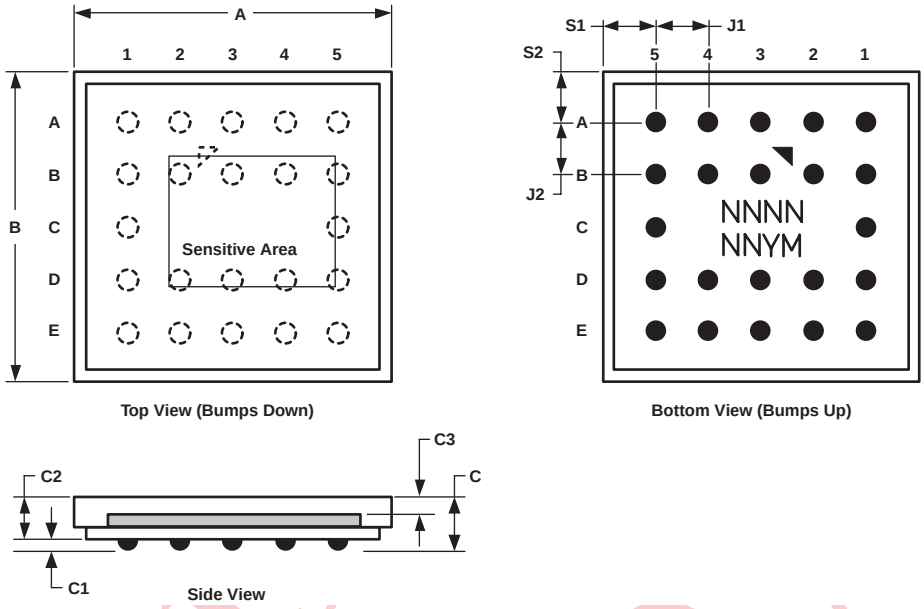
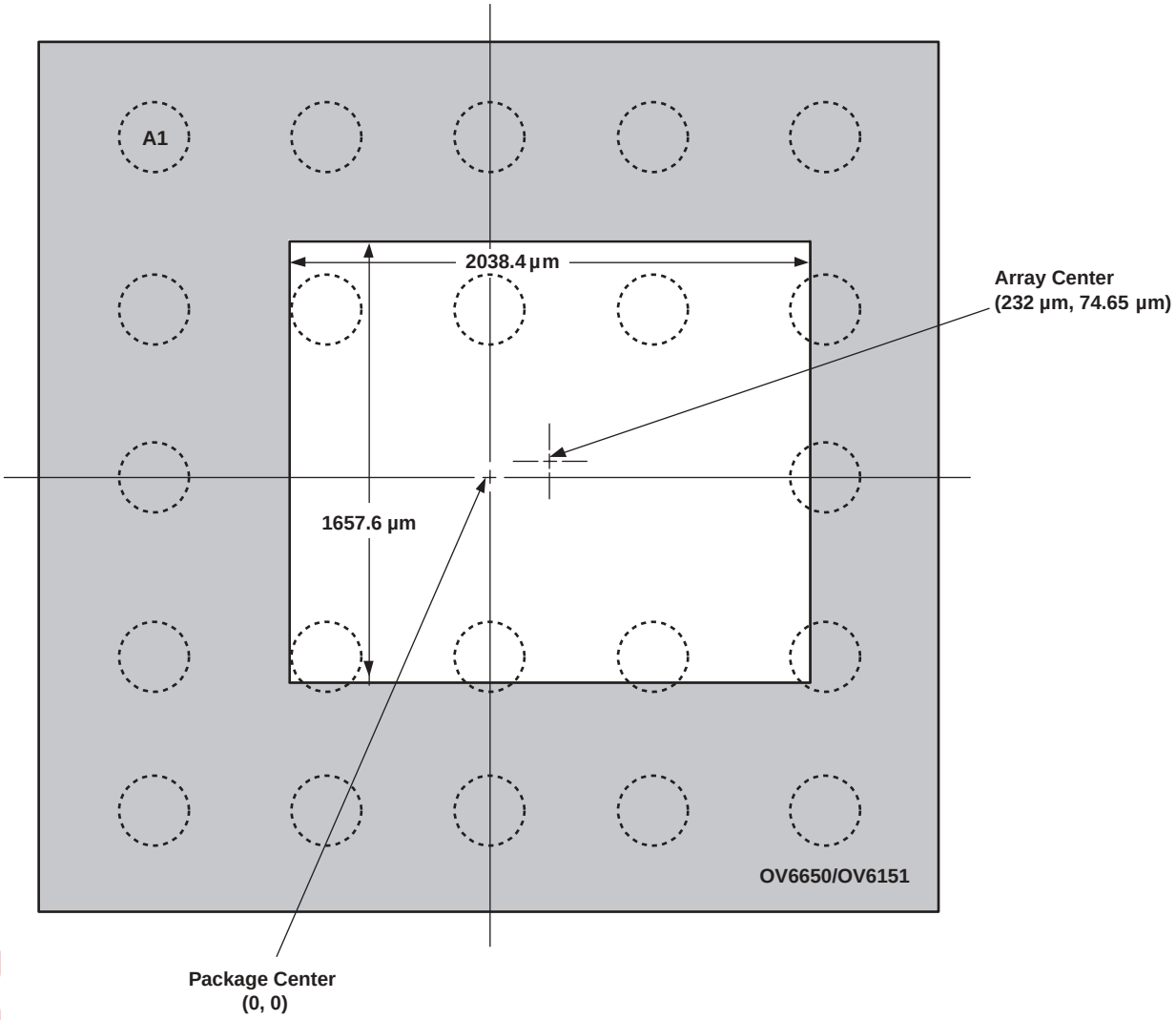


Table 6 CSP Package Dimensions

Parameter	Symbol	Minimum	Nominal	Maximum	Unit
Package Body Dimension X	A	3400	3425	3450	µm
Package Body Dimension Y	B	3460	3485	3510	µm
Package Height	C	740	800	860	µm
Ball Height	C1	130	160	190	µm
Package Body Thickness	C2	605	640	675	µm
Thickness of Glass Surface to Wafer	C3	400	415	430	µm
Ball Diameter	D	270	300	330	µm
Total Pin Count	N		22		
Pin Count X-axis	N1		5		µm
Pin Count Y-axis	N2		5		µm
Pins Pitch X-axis	J1		640		µm
Pins Pitch Y-axis	J2		640		µm
Edge-to-Pin Center Distance Analog X	S1	402.5	432.5	462.5	µm
Edge-to-Pin Center Distance Analog Y	S2	432.5	462.5	492.5	µm

Sensor Array Center

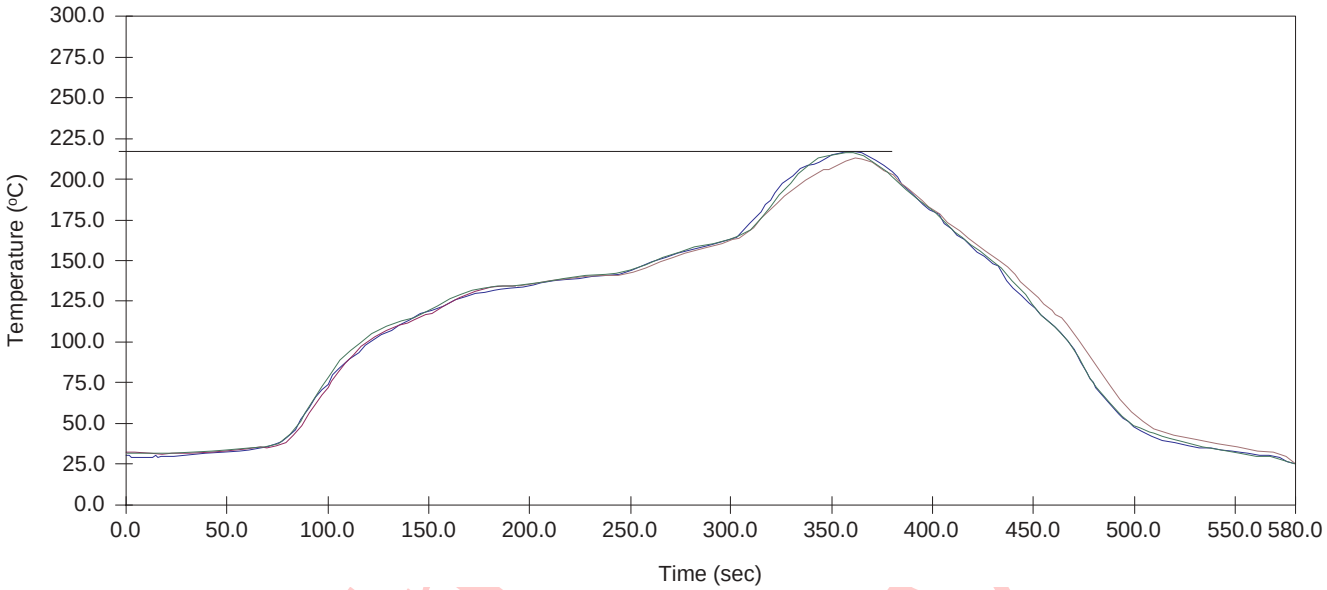
Figure 9 OV6650/OV6151 Sensor Array Center



Note: Due to the lens inversion, in order for the image to be right-side up, the OV6650/OV6151 must be mounted Pin 1 down.

IR Reflow Ramp Rate Requirements

Figure 10 IR Reflow Ramp Rate Requirements



Peak Temperature(°C)	Peak Time (sec)	≥ 100°C Time (sec)	≥ 150°C Time (sec)	≥ 190°C Time (sec)
216.7	358.00	347.00	167.00	70.00

Environmental Specifications

Table 7 OV6650/OV6151 Reliability Test Results

Parameter	Test Condition
Temperature/Humidity	85°C/85% Relative Humidity, 1000 hrs.[a]
Temperature Cycling (Air-to-Air)	-25°C / +125°C, 72 cycles/day, 1000 cycles[a]
Highly Accelerated Stress Test (HAST)	110°C / 85% Relative Humidity, 168 hrs.[a]
High Temperature Storage (HTS)	150°C, 1000 hrs.[a]
High Temperature Static Bias (HTSB)	125°C, 1000 hrs.[a]

a. Pre-Condition (Moisture Level II): 125°C, 24h → 85°C/60% RH/168h → IR Reflow 235°C, 10 sec, 3 cycles

Note:

- *All information shown herein is current as of the revision and publication date. Please refer to the OmniVision web site (http://www.ovt.com) to obtain the current versions of all documentation.*

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